Data Sheet | March 16, 2006 | FN8126.2

CPU Supervisor with 4K SPI EEPROM

These devices combine four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock Protect Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor executes code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the minimum V_{CC} trip point. $\overline{\text{RESET}}$/RESET is asserted until V_{CC} returns to proper operating level and stabilizes. Four industry standard V_{TRIP} thresholds are available, however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.

The memory portion of the device is a CMOS Serial EEPROM array with Intersil's block lock protection. The array is internally organized as 512 x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Intersil's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

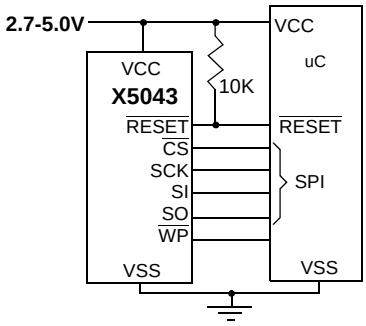
Features

- Low V_{CC} Detection and Reset Assertion
  - Four standard reset threshold voltages 4.63V, 4.38V, 2.93V, 2.63V
  - Re-program low V_{CC} reset threshold voltage using special programming sequence.
  - Reset signal valid to V_{CC} = 1V
- Selectable Time Out Watchdog Timer
- Long Battery Life with Low Power Consumption
  - <50µA max standby current, watchdog on
  - <10µA max standby current, watchdog off
- 4Kbits of EEPROM–1M Write Cycle Endurance
- Save Critical Data with Block Lock™ Memory
  - Protect 1/4, 1/2, all or none of EEPROM array
- Built-in Inadvertent Write Protection
  - Write enable latch
  - Write protect pin
- SPI Interface - 3.3MHz Clock Rate
- Minimize Programming Time
  - 16-byte page write mode
  - 5ms write cycle time (typical)
- Available Packages
  - 8 Ld MSOP, 8 Ld SOIC, 8 Ld PDIP
  - 14 Ld TSSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

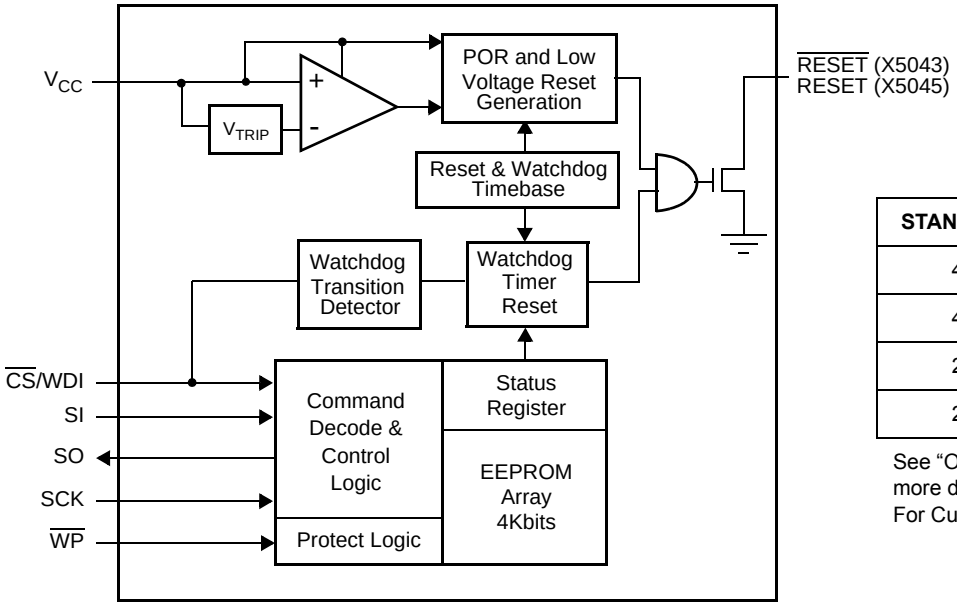
Applications

- Communications Equipment
  - Routers, Hubs, Switches
  - Set Top Boxes
- Industrial Systems
  - Process Control
  - Intelligent Instrumentation
- Computer Systems
  - Desktop Computers
  - Network Servers
- Battery Powered Equipment

Typical Application



Block Diagram



X5043, X5045

STANDARD V_{TRIP} LEVEL	SUFFIX
4.63V (+/-2.5%)	-4.5A
4.38V (+/-2.5%)	-4.5
2.93V (+/-2.5%)	-2.7A
2.63V (+/-2.5%)	-2.7

See “Ordering Information” on page 3. for more details
For Custom Settings, call Intersil.

Ordering Information

PART NUMBER RESET (ACTIVE LOW)	PART MARKING	PART NUMBER RESET (ACTIVE HIGH)	PART MARKING	V_{CC} RANGE	V_{TRIP} RANGE	TEMP RANGE (°C)	PACKAGE
X5043P-4.5A	X5043P AL	X5045P-4.5A	X5045P AL	4.5-5.5V	4.5-4.75	0 to 70	8 Ld PDIP
X5043PZ-4.5A (Note)	X5043P Z AL	X5045PZ-4.5A (Note)	X5045P Z AL			0 to 70	8 Ld PDIP (Pb-free)
X5043PI-4.5A	X5043P AM	X5045PI-4.5A	X5045P AM			-40 to 85	8 Ld PDIP
X5043PIZ-4.5A (Note)	X5043P Z AM	X5045PIZ-4.5A (Note)	X5045P Z AM			-40 to 85	8 Ld PDIP (Pb-free)
X5043S8-4.5A	X5043 AL	X5045S8-4.5A	X5045 AL			0 to 70	8 Ld SOIC
X5043S8Z-4.5A (Note)	X5043 Z AL	X5045S8Z-4.5A (Note)	X5045 Z AL			0 to 70	8 Ld SOIC (Pb-free)
X5043S8I-4.5A*	X5043 AM	X5045S8I-4.5A*	X5045 AM			-40 to 85	8 Ld SOIC
X5043S8IZ-4.5A* (Note)	X5043 Z AM	X5045S8IZ-4.5A* (Note)	X5045 Z AM			-40 to 85	8 Ld SOIC (Pb-free)
X5043M8-4.5A	AEM	X5045M8-4.5A	AEV			0 to 70	8 Ld MSOP
X5043M8Z-4.5A (Note)	DBS	X5045M8Z-4.5A (Note)	DCB			0 to 70	8 Ld MSOP (Pb-free)
X5043M8I-4.5A	AEN	X5045M8I-4.5A	AEW			-40 to 85	8 Ld MSOP
X5043M8IZ-4.5A (Note)	DBM	X5045M8IZ-4.5A (Note)	DBX			-40 to 85	8 Ld MSOP (Pb-free)
X5043V14I-4.5A	X5043V AM	X5045V14I-4.5A	X5045V AM			-40 to 85	14 Ld TSSOP
X5043V14IZ-4.5A (Note)	X5043V Z AM	X5045V14IZ-4.5A (Note)	X5045V Z AM			-40 to 85	14 Ld TSSOP (Pb-free)
X5043P	X5043P	X5045P	X5045P		4.25-4.5	0 to 70	8 Ld PDIP
X5043PZ (Note)	X5043P Z	X5045PZ (Note)	X5045P Z			0 to 70	8 Ld PDIP (Pb-free)
X5043PI	X5043P I	X5045PI	X5045P I			-40 to 85	8 Ld PDIP
X5043PIZ (Note)	X5043P Z I	X5045PIZ (Note)	X5045P Z I			-40 to 85	8 Ld PDIP (Pb-free)
X5043S8*	X5043	X5045S8*	X5045			0 to 70	8 Ld SOIC
X5043S8Z* (Note)	X5043 Z	X5045S8Z* (Note)	X5045 Z			0 to 70	8 Ld SOIC (Pb-free)
X5043S8I*	X5043 I	X5045S8I*	X5045 I			-40 to 85	8 Ld SOIC
X5043S8IZ* (Note)	X5043 Z I	X5045S8IZ* (Note)	X5045 Z I			-40 to 85	8 Ld SOIC (Pb-free)
X5043M8	AEO	X5045M8	AEX			0 to 70	8 Ld MSOP
X5043M8Z (Note)	DBN	X5045M8Z (Note)	DBY			0 to 70	8 Ld MSOP (Pb-free)
X5043M8I	AEP	X5045M8I	AEY			-40 to 85	8 Ld MSOP
X5043M8IZ (Note)	DBJ	X5045M8IZ (Note)	DBT			-40 to 85	8 Ld MSOP (Pb-free)
X5043V14I	X5043V I	X5045V14I	X5045V I			-40 to 85	14 Ld TSSOP
X5043V14IZ (Note)	X5043V Z I	X5045V14IZ (Note)	X5045V Z I			-40 to 85	14 Ld TSSOP (Pb-free)

Ordering Information (Continued)

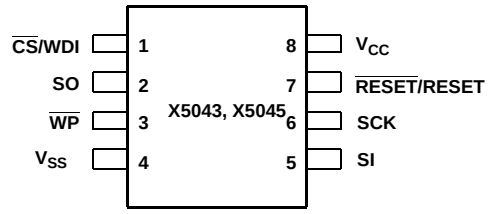
PART NUMBER RESET (ACTIVE LOW)	PART MARKING	PART NUMBER RESET (ACTIVE HIGH)	PART MARKING	V_{CC} RANGE	V_{TRIP} RANGE	TEMP RANGE (°C)	PACKAGE
X5043P-2.7A	X5043P AN	X5045P-2.7A	X5045P AN	2.7-5.5V	2.85-3.0	0 to 70	8 Ld PDIP
X5043PZ-2.7A (Note)	X5043P Z AN	X5045PZ-2.7A (Note)	X5045P Z AN			0 to 70	8 Ld PDIP (Pb-free)
X5043PI-2.7A	X5043P AP	X5045PI-2.7A	X5045P AP			-40 to 85	8 Ld PDIP
X5043PIZ-2.7A (Note)	X5043P Z AP	X5045PIZ-2.7A (Note)	X5045P Z AP			-40 to 85	8 Ld PDIP (Pb-free)
X5043S8-2.7A*	X5043 AN	X5045S8-2.7A	X5045 AN			0 to 70	8 Ld SOIC
X5043S8Z-2.7A* (Note)	X5043 Z AN	X5045S8Z-2.7A (Note)	X5045 Z AN			0 to 70	8 Ld SOIC (Pb-free)
X5043S8I-2.7A*	X5043 AP	X5045S8I-2.7A	X5045 AP			-40 to 85	8 Ld SOIC
X5043S8IZ-2.7A* (Note)	X5043 Z AP	X5045S8IZ-2.7A (Note)	X5045 Z AP			-40 to 85	8 Ld SOIC (Pb-free)
X5043M8-2.7A*	AEQ	X5045M8-2.7A	AEZ			0 to 70	8 Ld MSOP
X5043M8Z-2.7A (Note)	DBR	X5045M8Z-2.7A (Note)	DCA			0 to 70	8 Ld MSOP (Pb-free)
X5043M8I-2.7A*	AER	X5045M8I-2.7A	AFA			-40 to 85	8 Ld MSOP
X5043M8IZ-2.7A* (Note)	DBL	X5045M8IZ-2.7A (Note)	DBW			-40 to 85	8 Ld MSOP (Pb-free)
X5043V14I-2.7A	X5043V AP	X5045V14I-2.7A	X5045V AP			-40 to 85	14 Ld TSSOP
X5043V14IZ-2.7A (Note)	X5043V Z AP	X5045V14IZ-2.7A (Note)	X5045V Z AP			-40 to 85	14 Ld TSSOP (Pb-free)
X5043P-2.7	X5043P F	X5045P-2.7	X5045P F		2.55-2.7	0 to 70	8 Ld PDIP
X5043PZ-2.7 (Note)	X5043P Z F	X5045PZ-2.7 (Note)	X5045P Z F			0 to 70	8 Ld PDIP (Pb-free)
X5043PI-2.7	X5043P G	X5045PI-2.7	X5045P G			-40 to 85	8 Ld PDIP
X5043PIZ-2.7 (Note)	X5043P Z G	X5045PIZ-2.7 (Note)	X5045P Z G			-40 to 85	8 Ld PDIP (Pb-free)
X5043S8-2.7*	X5043 F	X5045S8-2.7*	X5045 F			0 to 70	8 Ld SOIC
X5043S8Z-2.7* (Note)	X5043 Z F	X5045S8Z-2.7* (Note)	X5045 Z F			0 to 70	8 Ld SOIC (Pb-free)
X5043S8I-2.7*	X5043 G	X5045S8I-2.7*	X5045 G			-40 to 85	8 Ld SOIC
X5043S8IZ-2.7* (Note)	X5043 Z G	X5045S8IZ-2.7* (Note)	X5045 Z G			-40 to 85	8 Ld SOIC (Pb-free)
X5043M8-2.7	AES	X5045M8-2.7	AFB			0 to 70	8 Ld MSOP
X5043M8Z-2.7 (Note)	DBP	X5045M8Z-2.7 (Note)	DBZ			0 to 70	8 Ld MSOP (Pb-free)
X5043M8I-2.7*	AET	X5045M8I-2.7	AFC			-40 to 85	8 Ld MSOP
X5043M8IZ-2.7* (Note)	DBK	X5045M8IZ-2.7 (Note)	DBU			-40 to 85	8 Ld MSOP (Pb-free)
X5043V14I-2.7	X5043V G	X5045V14I-2.7	X5045V G			-40 to 85	14 Ld TSSOP
X5043V14IZ-2.7 (Note)	X5043V Z G	X5045V14IZ-2.7 (Note)	X5045V Z G			-40 to 85	14 Ld TSSOP (Pb-free)

*Add "-T1" suffix for tape and reel.

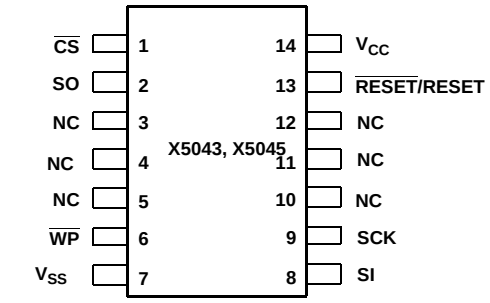
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

8 Ld SOIC/PDIP/MSOP



14 Ld TSSOP



Pin Descriptions

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin is latched on the rising edge of the clock input, while data on the SO pin changes after the falling edge of the clock input.

Chip Select ($\overline{CS}$/WDI)

When $\overline{CS}$ is high, the X5043, X5045 are deselected and the SO output pin is at high impedance and, unless an internal write operation is underway, the X5043, X5045 will be in the standby power mode. $\overline{CS}$ low enables the X5043, X5045, placing it in the active power mode. It should be noted that after power-up, a high to low transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

When $\overline{WP}$ is low, nonvolatile writes to the X5043, X5045 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held high, all functions, including non volatile writes operate normally. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the X5043, X5045. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no affect on a write.

Reset ($\overline{RESET}$, RESET)

X5043, X5045, $\overline{RESET}$/RESET is an active low/HIGH, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 200ms. $\overline{RESET}$/RESET also goes active if the Watchdog timer is enabled and $\overline{CS}$ remains either high or low longer than the Watchdog time out period. A falling edge of $\overline{CS}$ will reset the watchdog timer.

Pin Names

SYMBOL	DESCRIPTION
$\overline{CS}$/WDI	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
WP	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{RESET}$/RESET	Reset Output

Principles of Operation

Power-on Reset

Application of power to the X5043, X5045 activate a Power-on Reset Circuit. This circuit pulls the $\overline{RESET}$/RESET pin active. $\overline{RESET}$/RESET prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When V_{CC} exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{RESET}$/RESET, allowing the processor to begin executing code.

Low Voltage Monitoring

During operation, the X5043, X5045 monitor the V_{CC} level and asserts $\overline{RESET}$/RESET if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{RESET}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$/RESET signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

Watchdog Timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the WDI input. The microprocessor must toggle the $\overline{CS}$/WDI pin periodically to prevent an active $\overline{RESET}$/RESET signal. The $\overline{CS}$/WDI pin must be toggled from HIGH to LOW prior to the expiration of the watchdog time out period. The state of two nonvolatile control bits in the Status Register determines the watchdog timer period. The microprocessor can change these watchdog bits. With

no microprocessor action, the watchdog timer control bits remain unchanged, even during total power failure.

V_{CC} Threshold Reset Procedure

The X5043, X5045 are shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X5043, X5045 threshold may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and tie the $\overline{WP}$ pin to the programming voltage V_P. Then send a WREN command, followed by a write of Data 00h to address 01h. $\overline{CS}$ going HIGH on the write operation initiates the V_{TRIP} programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

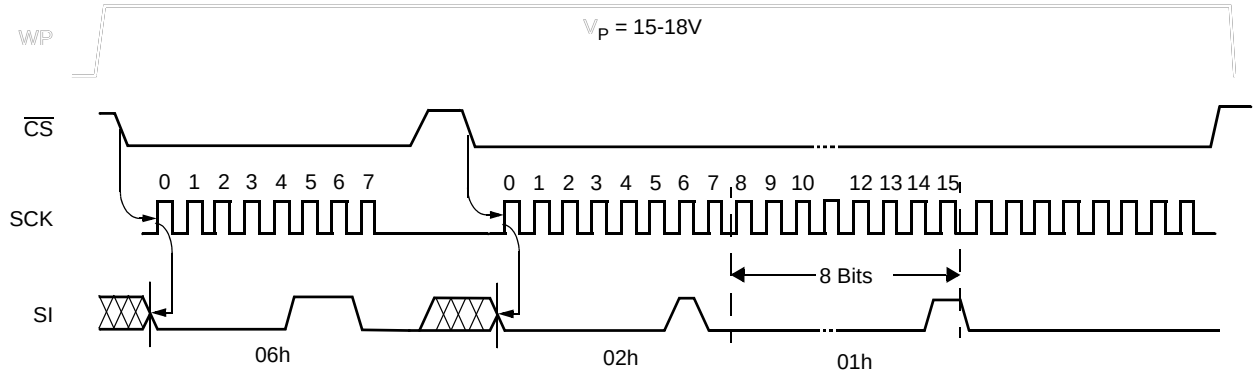
Note: This operation also writes 00h to array address 01h.

Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a “native” voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the V_{TRIP} voltage, apply at least 3V to the V_{CC} pin and tie the $\overline{WP}$ pin to the programming voltage V_P. Then send a WREN command, followed by a write of Data 00h to address 03h. $\overline{CS}$ going HIGH on the write operation initiates the V_{TRIP} programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

Note: This operation also writes 00h to array address 03h.



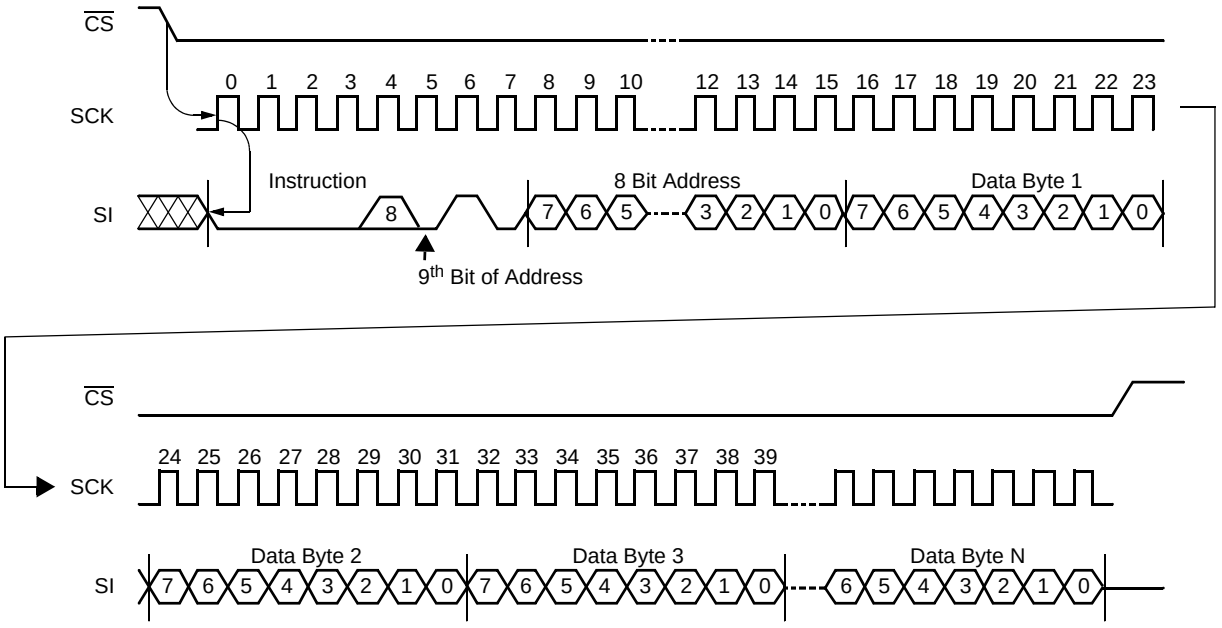


FIGURE 9. WRITE MEMORY SEQUENCE

Operational Notes

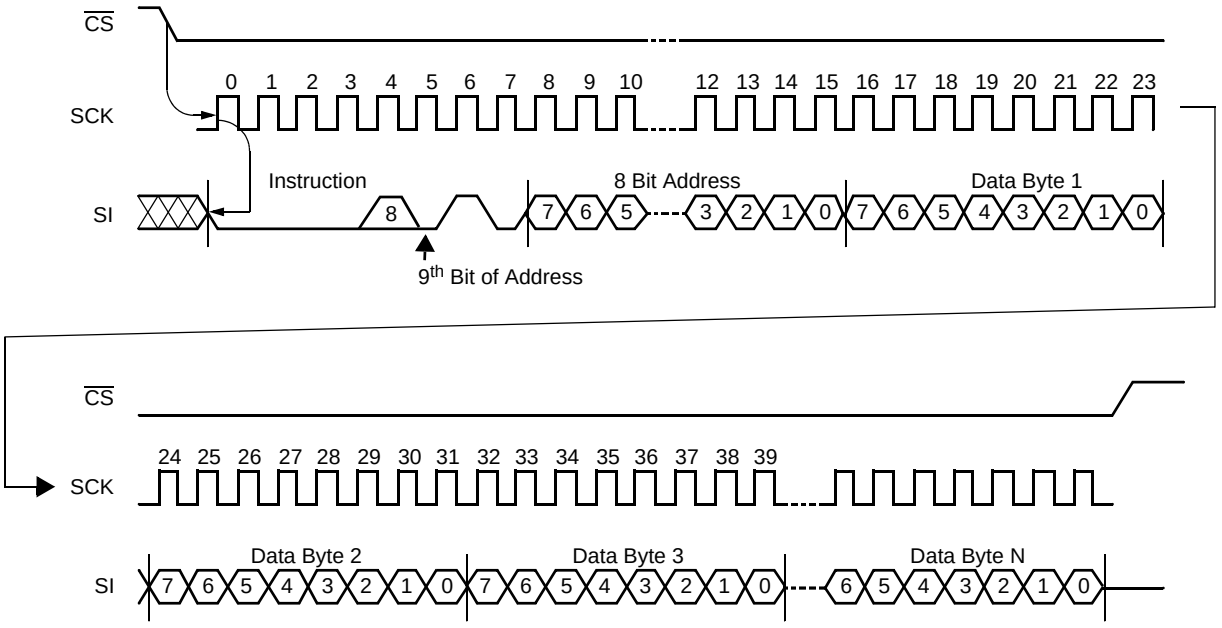
The device powers-up in the following state:

1. The device is in the low power standby state.
2. A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
3. SO pin is high impedance.
4. The Write Enable Latch is reset.
5. The Flag Bit is reset.
6. Reset Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.
- Block Protect bits provide additional level of write protection for the memory array.
- The $\overline{WP}$ pin LOW blocks nonvolatile write operations.



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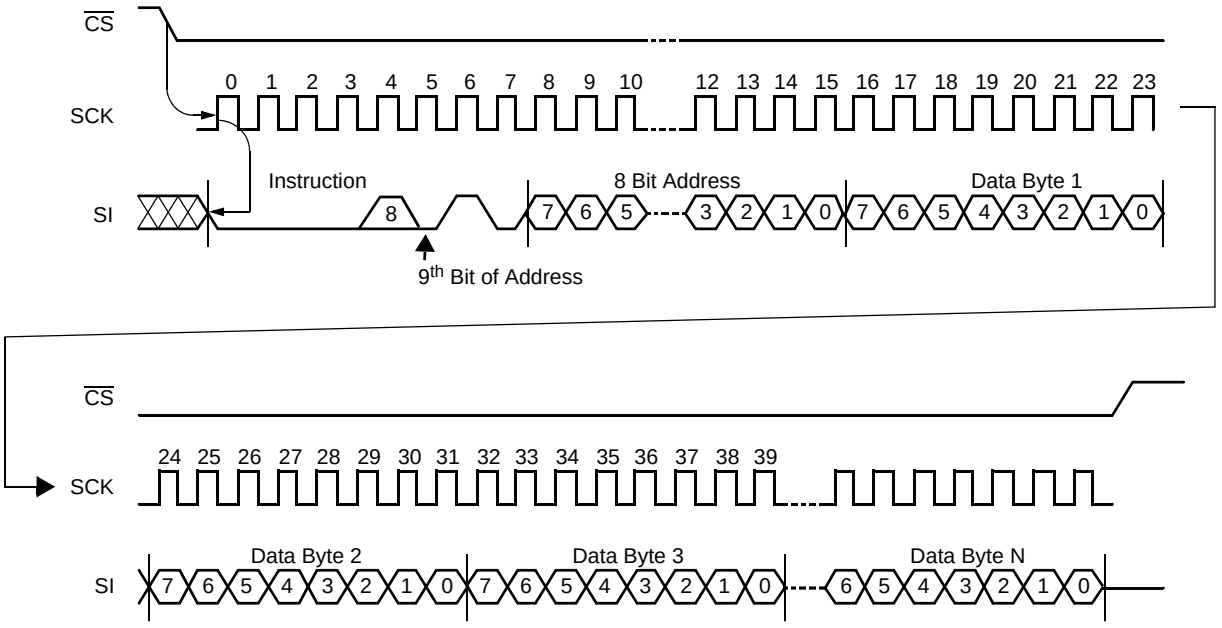

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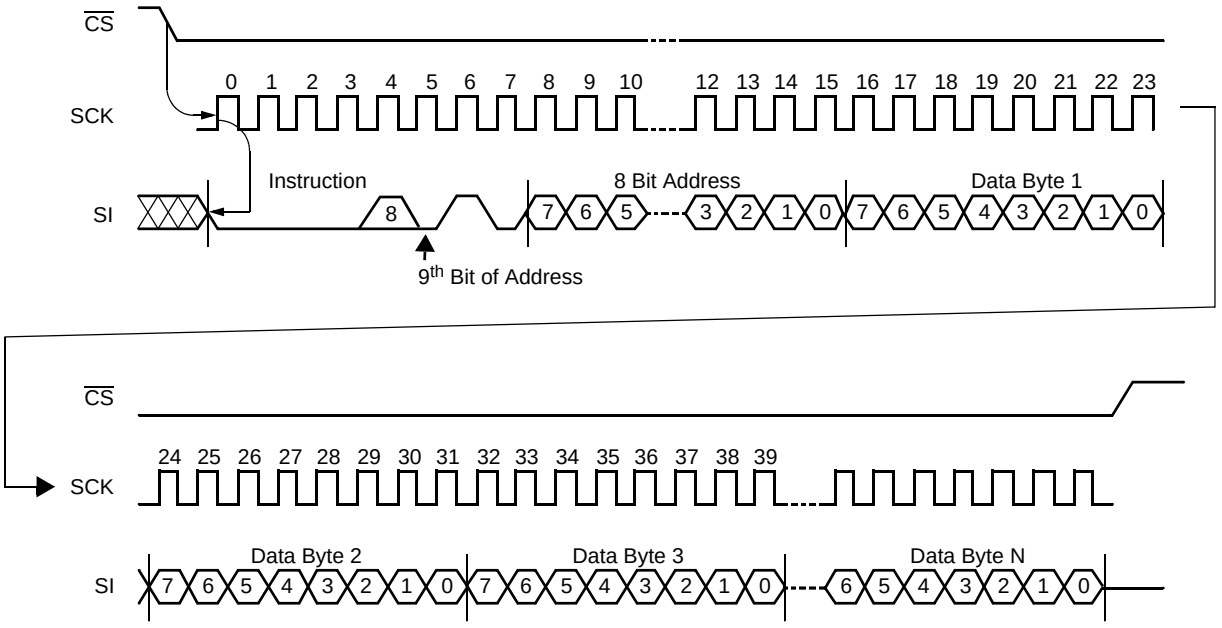

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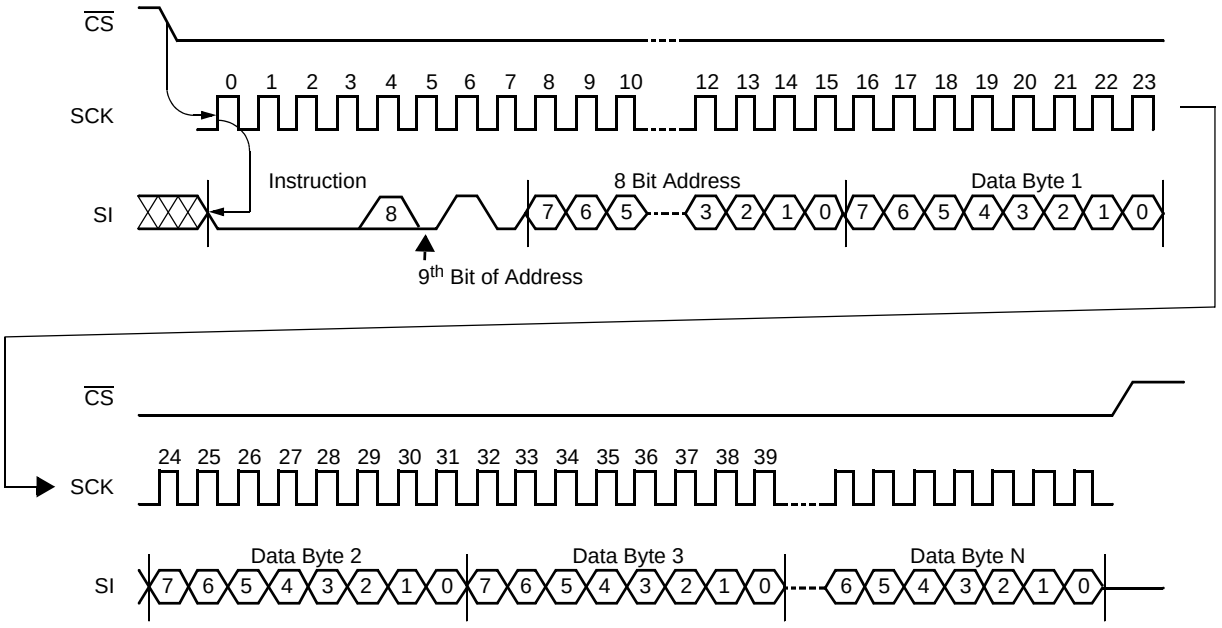

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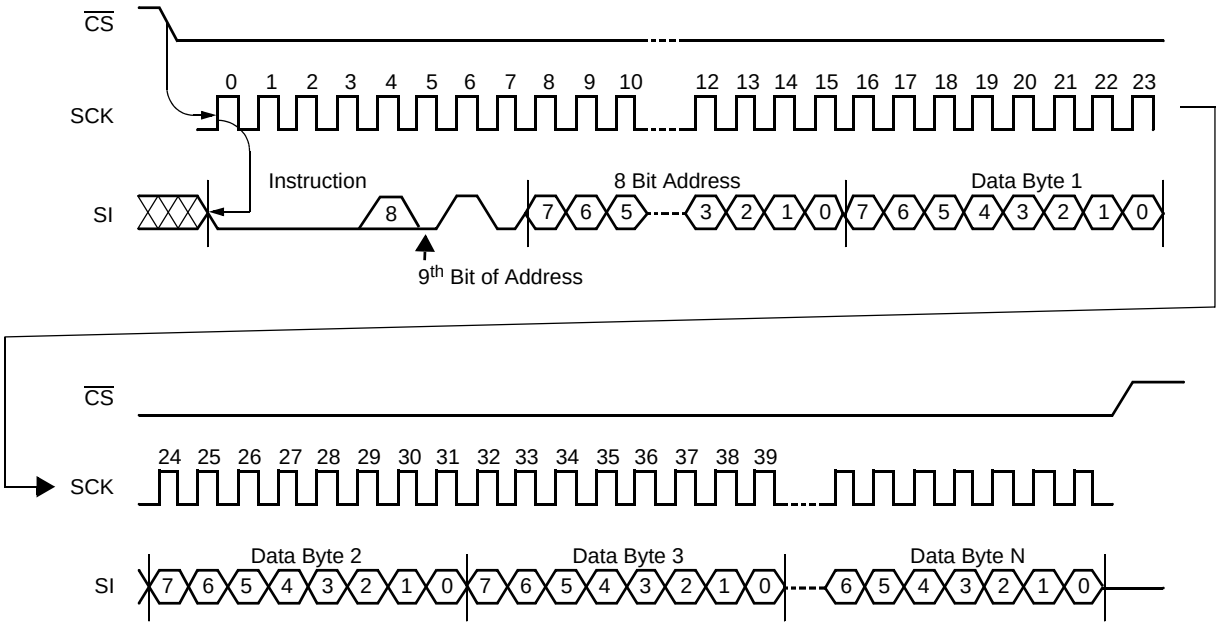

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Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.
- Block Protect bits provide additional level of write protection for the memory array.
- The $\overline{WP}$ pin LOW blocks nonvolatile write operations.

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any pin with
respect to V_{SS} . . . . . -1.0V to +7V
D.C. output current. 5mA
Lead temperature (soldering, 10 seconds) . . . . . 300°C

Recommended Operating Conditions

Temperature:
Commercial. . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage:
-2.7, -2.7A . . . . . 2.7V to 5.5V
Blank, -4.5A . . . . . 4.5V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Specifications (Over the recommended operating conditions unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS/COMMENTS	LIMITS			UNIT
			MIN	TYP(2)	MAX	
I_{CC1}	V_{CC} Write Current (Active)	SCK = 3.3MHz(3); SO, $\overline{RESET}$, RESET = Open			3	mA
I_{CC2}	V_{CC} Read Current (Active)	SCK = 3.3MHz(3); SI = V_{SS}, $\overline{RESET}$, RESET = Open			2	mA
I_{SB1}	V_{CC} Standby Current WDT = OFF	$\overline{CS}$ = V_{CC}, SCK, SI = V_{SS}, V_{CC} = 5.5V			10	µA
I_{SB2}	V_{CC} Standby Current WDT = ON	$\overline{CS}$ = V_{CC}, SCK, SI = V_{SS}, V_{CC} = 5.5V			50	µA
I_{LI}	Input Leakage Current	SCK, SI, WP = V_{SS} to V_{CC}		0.1	10	µA
I_{LO}	Output Leakage Current	SO, $\overline{RESET}$, RESET = V_{SS} to V_{CC}		0.1	10	µA
V_{IL}(1)	Input LOW Voltage	SCK, SI, $\overline{WP}$, $\overline{CS}$	-0.5		V_{CC} x 0.3	V
V_{IH}(1)	Input HIGH Voltage	SCK, SI, $\overline{WP}$, $\overline{CS}$	V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage (SO)	I_{OL} = 2mA @ V_{CC} = 2.7V I_{OL} = 0.5mA @ V_{CC} = 1.8V			0.4	V
V_{OH1}	Output HIGH Voltage (SO)	V_{CC} > 3.3V, I_{OH} = –1.0mA	V_{CC} - 0.8			V
V_{OH2}	Output HIGH Voltage (SO)	2V < V_{CC} ≤ 3.3V, I_{OH} = –0.4mA	V_{CC} - 0.4			V
V_{OH3}	Output HIGH Voltage (SO)	V_{CC} ≤ 2V, I_{OH} = –0.25mA	V_{CC} - 0.2			V
V_{OLRS}	Output LOW Voltage ($\overline{RESET}$, RESET)	I_{OL} = 1mA			0.4	V

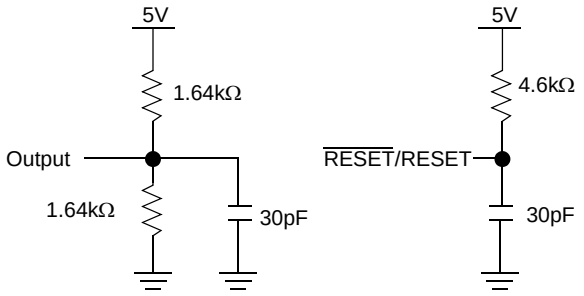
Capacitance T_A = +25°C, f = 1MHz, V_{CC} = 5V

SYMBOL	TEST	CONDITIONS	MAX	UNIT
C_{OUT}(2)	Output Capacitance (SO, $\overline{RESET}$, RESET)	V_{OUT} = 0V	8	pF
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	V_{IN} = 0V	6	pF

NOTES:

1. V_{IL} min. and V_{IH} max. are for reference only and are not tested.
2. This parameter is periodically sampled and not 100% tested.
3. SCK frequency measured from V_{CC} x 0.1/V_{CC} x 0.9

Equivalent A.C. Load Circuit at 5V V_{CC}



A.C. Test Conditions

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

AC Electrical Specifications (Over recommended operating conditions, unless otherwise specified)

SYMBOL	PARAMETER	2.7V–5.5V MIN	2.7V–5.5V MAX	UNIT
DATA INPUT TIMING				
f_{SCK}	Clock Frequency	0	3.3	MHz
t_{CYC}	Cycle Time	300		ns
t_{LEAD}	$\overline{CS}$ Lead Time	150		ns
t_{LAG}	$\overline{CS}$ Lag Time	150		ns
t_{WH}	Clock HIGH Time	130		ns
t_{WL}	Clock LOW Time	130		ns
t_{SU}	Data Setup Time	30		ns
t_H	Data Hold Time	30		ns
t_{RI}(4)	Input Rise Time		2	µs
t_{FI}(4)	Input Fall Time		2	µs
t_{CS}	$\overline{CS}$ Deselect Time	100		ns
t_{WC}(5)	Write Cycle Time		10	ms

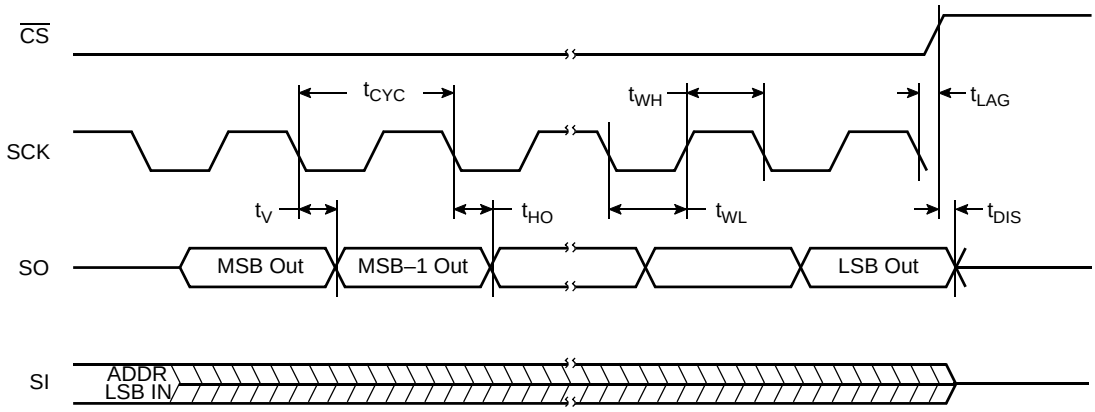
Data Output Timing

SYMBOL	PARAMETER	2.7–5.5V MIN	2.7–5.5V MAX	UNIT
f_{SCK}	Clock Frequency	0	3.3	MHz
t_{DIS}	Output Disable Time		150	ns
t_V	Output Valid from Clock Low		120	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		50	ns
t_{FO}(4)	Output Fall Time		50	ns

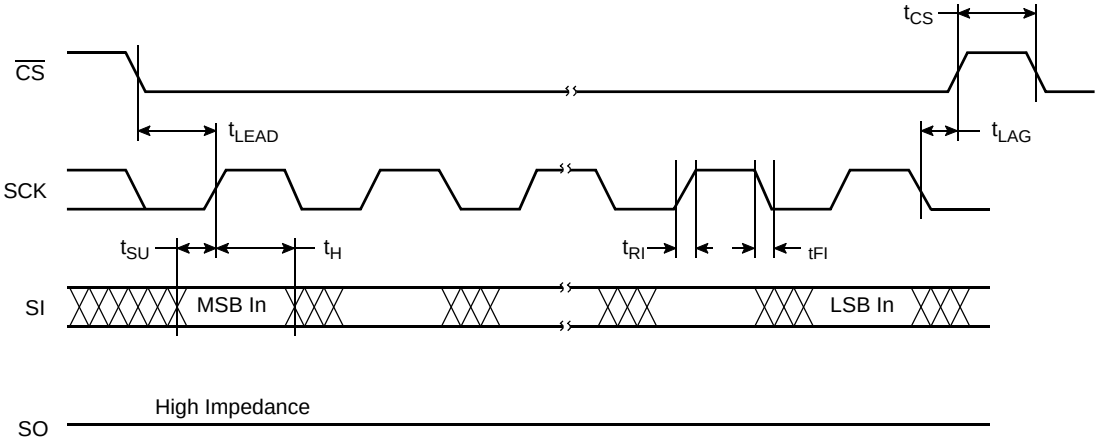
NOTES:

4. This parameter is periodically sampled and not 100% tested.
5. t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing



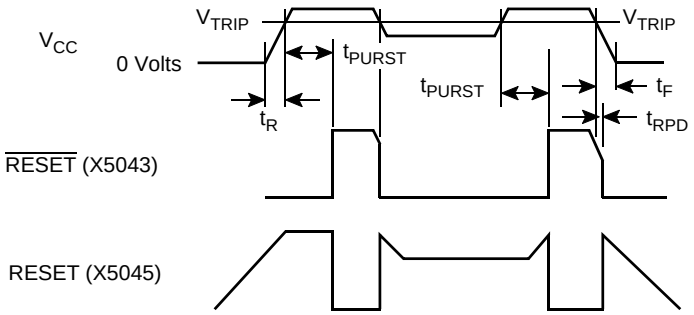
Serial Input Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Power-Up and Power-Down Timing



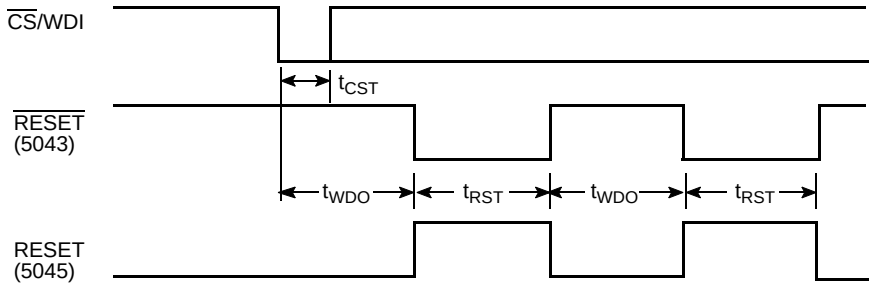
$\overline{RESET}$ Output Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{TRIP}	Reset Trip Point Voltage, (-4.5A) Reset Trip Point Voltage, (Blank) Reset Trip Point Voltage, (-2.7A) Reset Trip Point Voltage, (-2.7)	4.5 4.25 2.85 2.55	4.62 4.38 2.92 2.62	4.75 4.5 3.0 2.7	V
t_{PURST}	Power-up Reset Time Out	100	200	400	ms
t_{RPD}(6)	V_{CC} Detect to Reset/Output			500	ns
t_F(6)	V_{CC} Fall Time	10			µs
t_R(6)	V_{CC} Rise Time	0.1			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

NOTE:

6. This parameter is periodically sampled and not 100% tested.

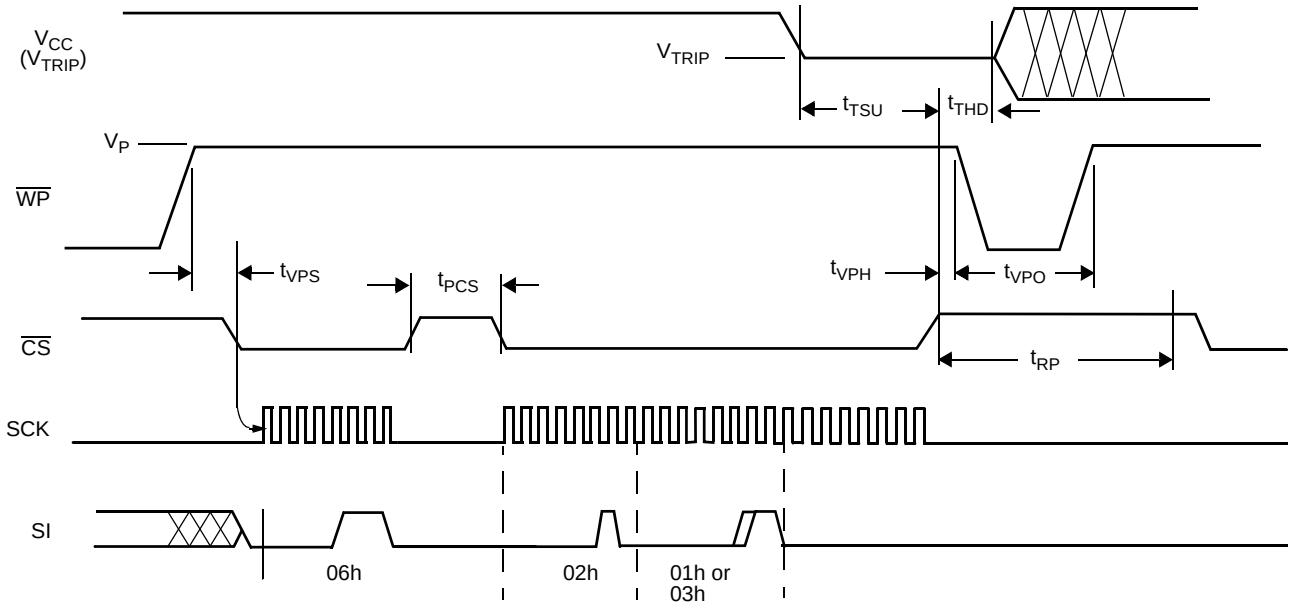
$\overline{CS}$/WDI vs. $\overline{RESET}$/RESET Timing



$\overline{RESET}$/RESET Output Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{WDO}	Watchdog Time Out Period, WD1 = 1, WD0 = 1 (default) WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 100 450 1	 OFF 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	$\overline{CS}$ Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Time Out	100	200	400	ms

V_{TRIP} Programming Timing Diagram



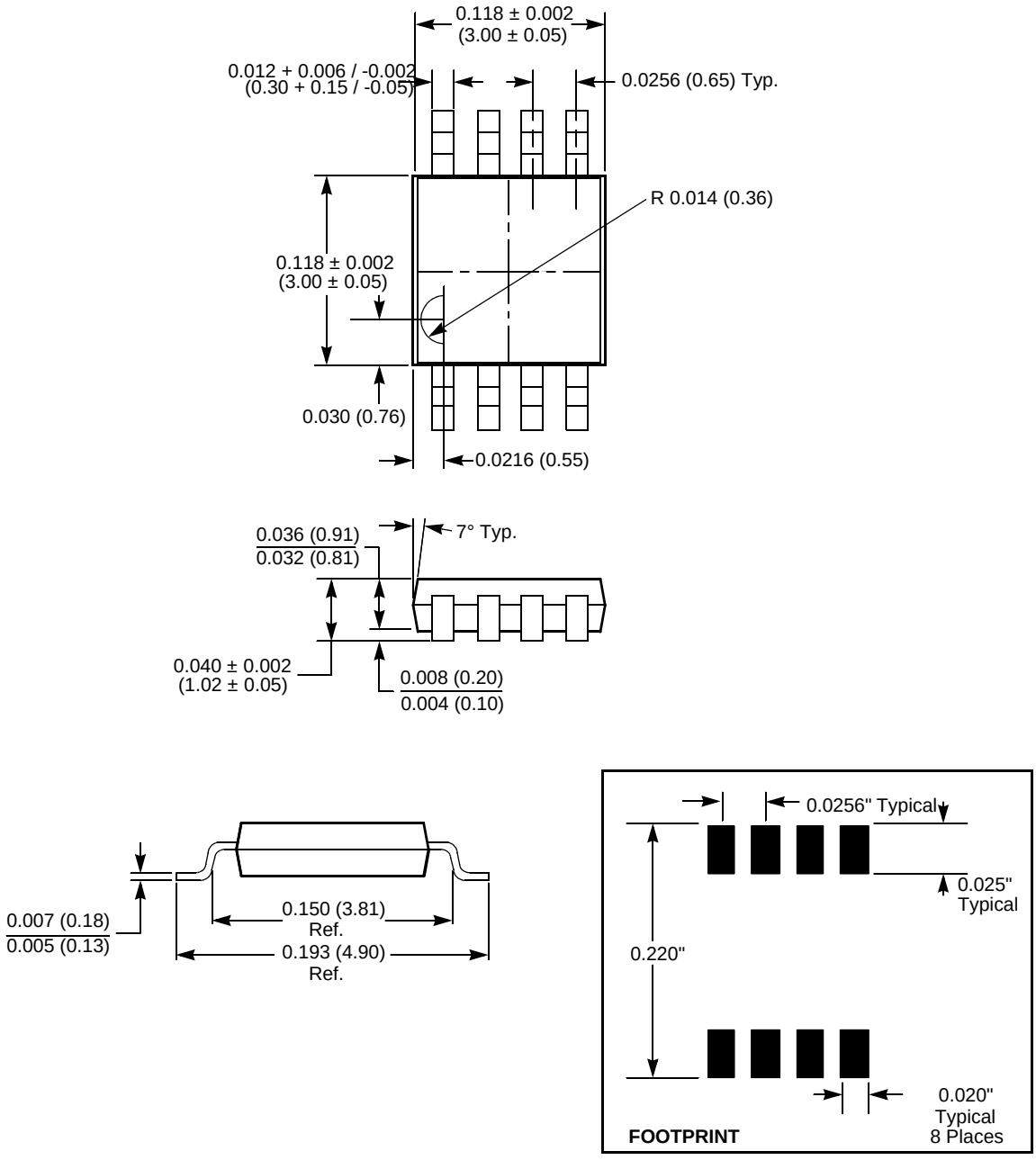
V_{TRIP} Programming Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{VPS}	V_{TRIP} Program Enable Voltage Setup time	1		µs
t_{VPH}	V_{TRIP} Program Enable Voltage Hold time	1		µs
t_{PCS}	V_{TRIP} Programming $\overline{CS}$ inactive time	1		µs
t_{TSU}	V_{TRIP} Setup time	1		µs
t_{THD}	V_{TRIP} Hold (stable) time	10		ms
t_{WC}	V_{TRIP} Write Cycle Time		10	ms
t_{VPO}	V_{TRIP} Program Enable Voltage Off time (Between successive adjustments)	0		µs
t_{RP}	V_{TRIP} Program Recovery Period (Between successive adjustments)	10		ms
V_P	Programming Voltage	15	18	V
V_{TRAN}	V_{TRIP} Programmed Voltage Range	1.7	4.75	V
V_{tv}	V_{TRIP} Program variation after programming (0-75°C). (Programmed at 25°C.)	-25	+25	mV

V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

Packaging Information

8-Lead Miniature Small Outline Gull Wing Package Type M

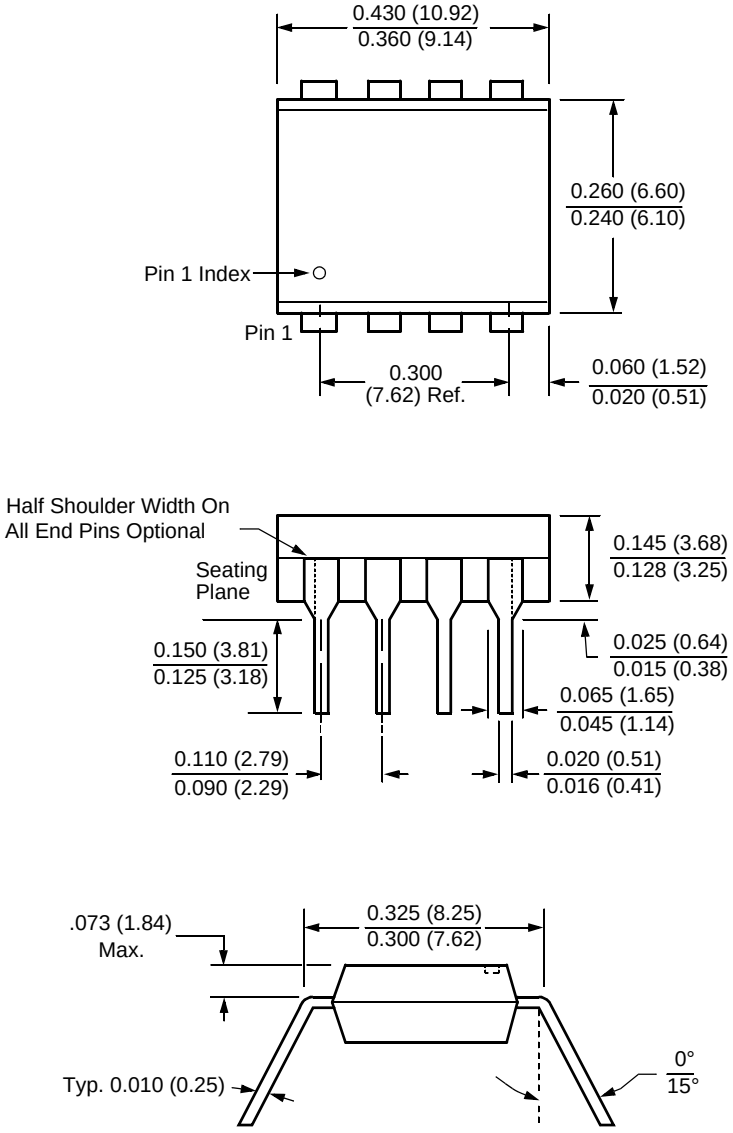


NOTE:

1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

Packaging Information

8-Lead Plastic Dual In-Line Package Type P



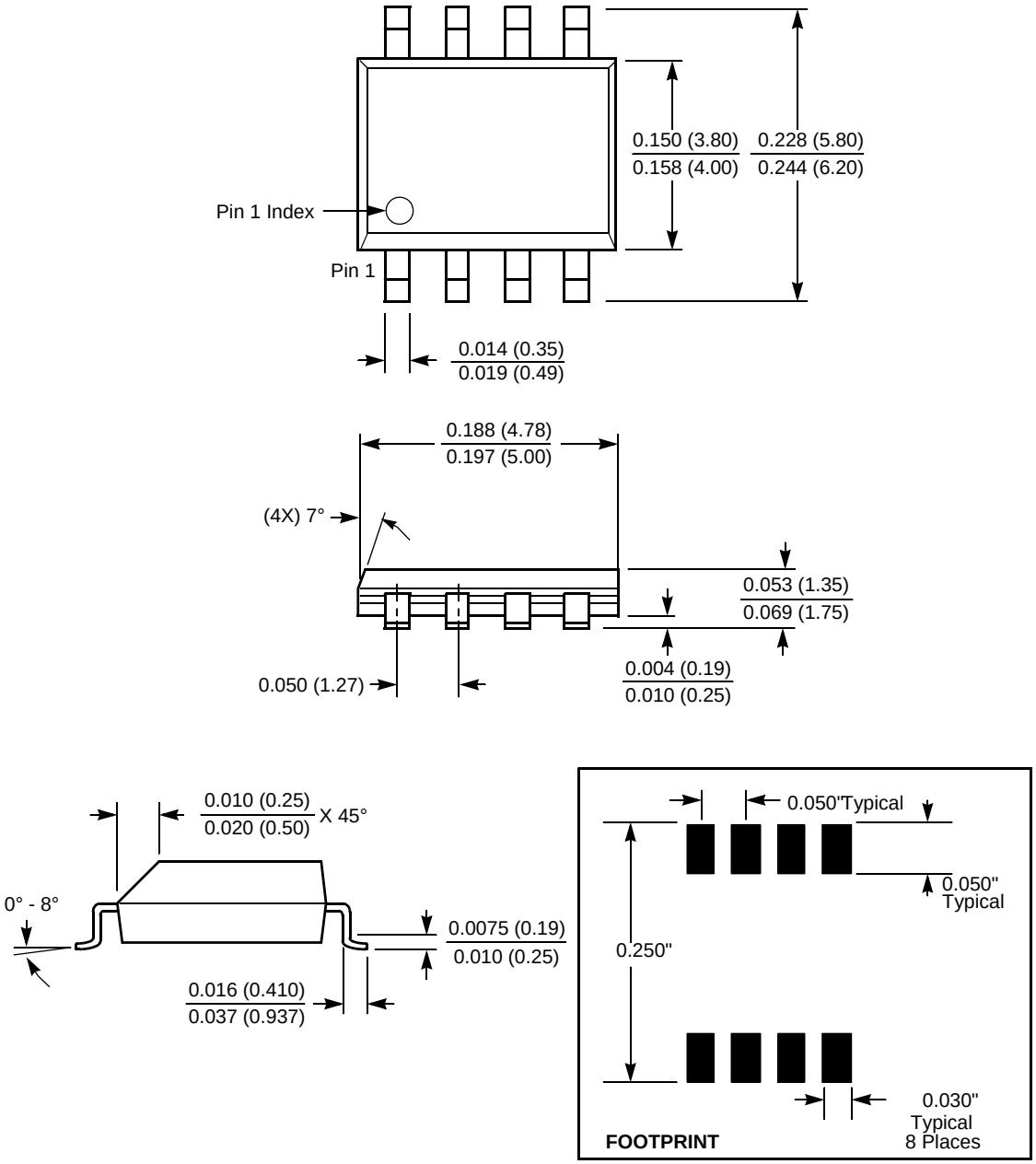
NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

Packaging Information

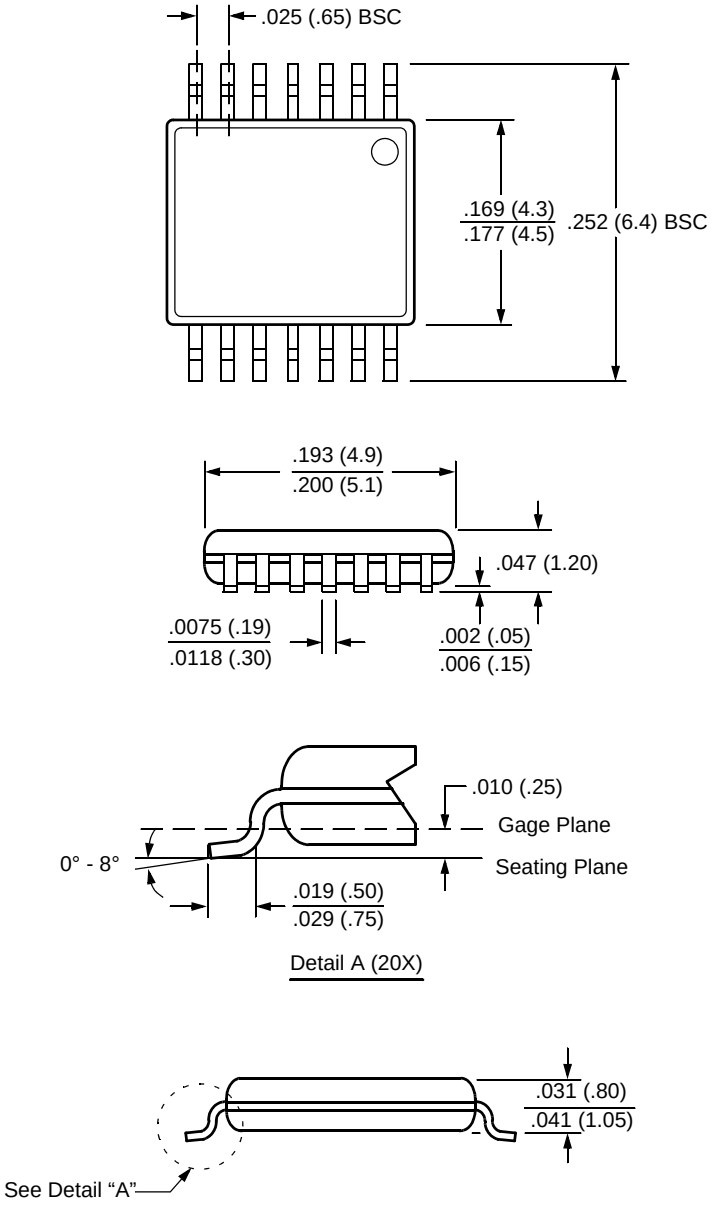
8-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

14-Lead Plastic, TSSOP, Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)